ABSTRACT OF THE DISCLOSURE

In a double-spacer or multi-spacer approach to the formation of sophisticated field effect transistors, an upper sidewall portion of a gate electrode may be effectively exposed during recessing of an outer spacer element, since the outer spacer is substantially comprised of the same material as the liner material. Consequently, the anisotropic etch process for recessing the outer sidewall spacer also efficiently removes liner residues on the upper sidewall portion and provides an increased diffusion path for a refractory metal. Additionally, the lateral extension of the silicide regions on the drain and source area may be increased by correspondingly controlling an isotropic etch process for removing oxide residues.